Accelerating the Data Plane
With the TILE-Mx Manycore Processor

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Announcing the World’s First
100-Core
64-Bit ARMv8 Processor

The TILE-Mx100 processor from EZchip

- Highest-performance manycore based on ARMv8
- Best power efficiency and compute density
- Optimized for networking and Network Functions Virtualization (NFV)
TILE-Mx100 Processor Highlights

- **World’s highest-performance manycore ARMv8 processor**
  - 100 cores, coherent cache, and external memory

- **5th generation SkyMesh™ coherent architecture**
  - Massive bandwidth and low latency
  - Application performance scales linearly

- **High-performance I/O and memory**
  - 1G, 10G, 25G, 40G, 50G, 100G Ethernet, Interlaken, PCIe 3.0
  - DDR4 memory system w/ ECC

- **State-of-the-art integrated networking accelerators**
  - Traffic manager, flow lookups, crypto, etc.
  - Delivered through standard software models and APIs
  - Supports DPDK and ODP with hardware acceleration

- **Standard ARM software ecosystem**
  - Easy software portability between x86 and ARM
  - Hypervisors (KVM, Xen, etc.), operating systems (Linux), and tools
Tile Processors Delivering on the Promise of Manycore

- ARMv8.0 Architecture
  - Full virtualization
  - Advanced acceleration
  - SkyMesh architecture

3rd-Generation Tile Architecture
- Cache-Coherent
- C-programmable
- Scalable

2nd-Generation
- iMesh Architecture

TILE-Pro
- 64/36 cores

TILE-Gx
- 72/36/16/9 cores

TILE-Mx
- 100/64/36 cores

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Markets & Applications

Carrier Routers
- L2-L3
- Load Balancing, Security, DPI, Net-Monitoring

Data Center & Enterprise Appliances
- Accelerating VNFs with Chips Blades Intelligent TOR Appliances
- Load Balancing, Security, DPI, Net-Monitoring

NFV & SDN
- Executing VNFs with Chips Blades Intelligent NICs NFV Servers

Enterprise Routers & Video
- Control & Data Planes, Voice & Video Encoding

Network Processors
- Data Plane 400Gbps-800Gbps
- Multicore Processors
- Data and Control Planes 10Gbps-200Gbps
TILE-Mx100 excels at L2–L7 deep-packet processing

- L2, L3 vSwitching
- Massive compute and threading support complex stateful flow processing
- Large cache and high-performance memory subsystem
- Traffic buffering, queueing, shaping, policing, QoS provisioning
- Pattern-match and signature search
- Crypto and compression acceleration
- Intelligent server adapter, blade, or appliance powered by the TILE-Mx processor
- Fast-path processing for networking functions enables higher VM density, and fewer servers & VMs to manage
- Increase the scale and reduce the cost & power of SDN/NFV
- Standard, familiar software environment
- 10G/25G/40G/50G/100G Ethernet interfaces
Optimized server platform for running virtualized networking functions (VNF)

- Wire-speed performance for workloads with heavy network processing
  - Classification, switch/route, encrypt/decrypt
  - OVS and overlays, service chaining, and flow migration
  - App. recognition, QoS, and SLA enforcement

Low power, high density
Network Functions Server
The TILE-Mx is carefully architected to deliver over 100Gbps of stateful packet processing.

**Hardware accelerators** handle the essential steps in the “life of the packet”:
- HW-based traffic management, statistics, and counters
- Flow lookups and packet ordering
- Programmable stateful packet distribution to cores
- Crypto and compression functions

Run your application code!
- On the highest performance many-core ARM, leveraging huge memory BW and the ARM software ecosystem
- Focus on your market-differentiation
TILE-Mx100 Key Features: Cores

- 100 ARM Cortex-A53 cores with multilevel cache
  - NEON™ 128b SIMD and floating-point acceleration
- SkyMesh™ architecture delivers full SMP with superior scalability
  - Fully cache-coherent scalable network-on-chip
- 40MB total on-chip cache
  - 3-level cache hierarchy (L1, L2, L3)
- Tile Core Accelerators (TCAs)
  - Close proximity to ARM cores for low latency
  - Accelerating inter-core messaging, fast lookups, and work scheduling
TILE-Mx100 Acceleration Features

- World’s leading Traffic Management (TM) engine
  - Wire-speed traffic shaping, policing, and QoS enforcement
  - 256K queues, 300Mpps, H-QoS with five scheduling levels

- mPIPE 3.0 programmable network front-end
  - Classification, packet distribution, buffer management
  - Checksum, LSO/RSS, statistics
  - Precision time stamping and IEEE 1588v2

- Accelerated lookup functions
  - LPM, ACL, flow lookups, and pattern search

- Crypto acceleration
  - IPsec, SSL, DTLS, SRTP – both symmetric and public key

- Statistics and atomic-flow table acceleration
  - Designed for low-overhead management of huge tables
TILE-Mx100 SkyMesh™

- 5th generation network on chip (NoC)
- Unified fabric provides low latency, high-bandwidth connectivity
  - 25Tbps of aggregate bandwidth
- Provides fully coherent communication among all on-chip components:
  - Caches, cores, accelerators, I/O, and memory
- Patented SkyMesh™ cache-coherence protocol improves on-chip data sharing
  - Lowers application latency and reduces DRAM bandwidth demand
ARMv8 architecture leverages vast ecosystem to speed development and enable software reuse

- Standard development tools
  - Compilers
  - Debuggers
  - Profilers
  - Chip Simulator

- Familiar runtime environment
  - Operating systems (Linux, BSD, VxWorks)
  - Hypervisors (KVM, etc.)
  - 3rd party network stacks (Wind, Inside)

- Rich applications
  - DPDK, OpenDataPlane
  - OvS
  - 3rd party DPI (QOSMOS, Procera)
Comprehensive Software Offering

Apps
- Linux/BSD/Win SNIC
- OCP Switch Acceleration
- OpenFlow
- L2/L3 Proc.
- Load Bal.
- Ipsec, SSL
- DPDK PMD
- App Recognition
- IPS/IDS
- OVS

Infrastructure
- OFtable
- Host net device
- Crypto
- ODP
- DPDK
- DPI

Platforms
- TILE-Mx SDK
- ZOL
- PCIe drivers
- Sim. lib
- Algo. lib

Platform Technologies
Software-Defined Network Appliance

- Packet classification & filtering
- Encaps/Decaps, load balancing
- DPI, Security

1RU SDN/NFV Appliance

TILE Mx100

100GE, 50GE, 25GE
40GE, 10GE, 1GE

DDR4

PCle Gen3

SATA/SAS Controller (RAID)

Disk
Software-Defined Network Adapter

- vSwitch
- Packet classification & filtering
- DPI
- Security offload
TILE-Mx - Summary

- **One hundred 64bit ARM CPU cores** in one chip for highest compute and best power/performance ratio

- **2D Mesh interconnect:** Massive bandwidth, low latency and linear scalability

- **Advanced networking hardware accelerators** for high-performance data path packet processing

- **Standard ARM ecosystem,** leveraging software from the open source community and for easy software portability between platforms

- **Empowering networking applications** including load balancing, security, network monitoring, NFV & SDN, application recognition and video processing

- **Target markets versatility:** Data center, cloud, enterprise and carrier networks serviced by network appliances, white boxes, NFV servers and application software vendors

- **Sampling 2H 2016**